ABSTRACT OF THE DISCLOSURE

The multilayer chip varistor of the present invention includes a varistor body including a plurality of varistor layers and inner electrodes arranged to sandwich each of the varistor layers, terminal electrodes formed on each ends of the varistor body and connected to the inner electrodes, and glass layers formed between the varistor body and the terminal electrodes. In addition, a plated layers and are formed on the surface of the terminal electrodes.